Laser testing and analysis of SEE in DDR3 memory components

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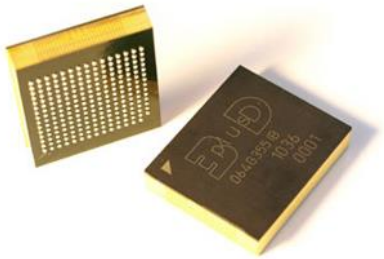
Context & Motivation

- Dynamic memories (DRAMs) widely used in space applications for mass storage

- DDR3 are now being considered for space applications in the coming years
  - Clock frequency up to 1066 MHz (2133 Mbps)
  - Capacity up to 8 Gb

- Interest for identification of a new radiation tolerant component in order to integrate it in space modules
  - DDR3L : Low power DDR3 interesting for energy saving at module level



What about DDR3L radiation effects sensitivity ?

➡ SEE, TID…

➡ Methodology optimization

➔ NSREC 2017 - “Analysis of Single-Event Effects in DDR3 and DDR3L SDRAMs using Laser Testing and Monte-Carlo simulations”

Outline

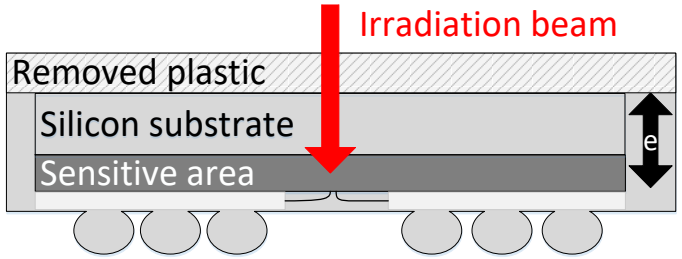
- Devices under study
- Experimental setup
- Laser testing results
- Monte-Carlo simulation
- Conclusion

Devices under study

- **DUTs specifications**

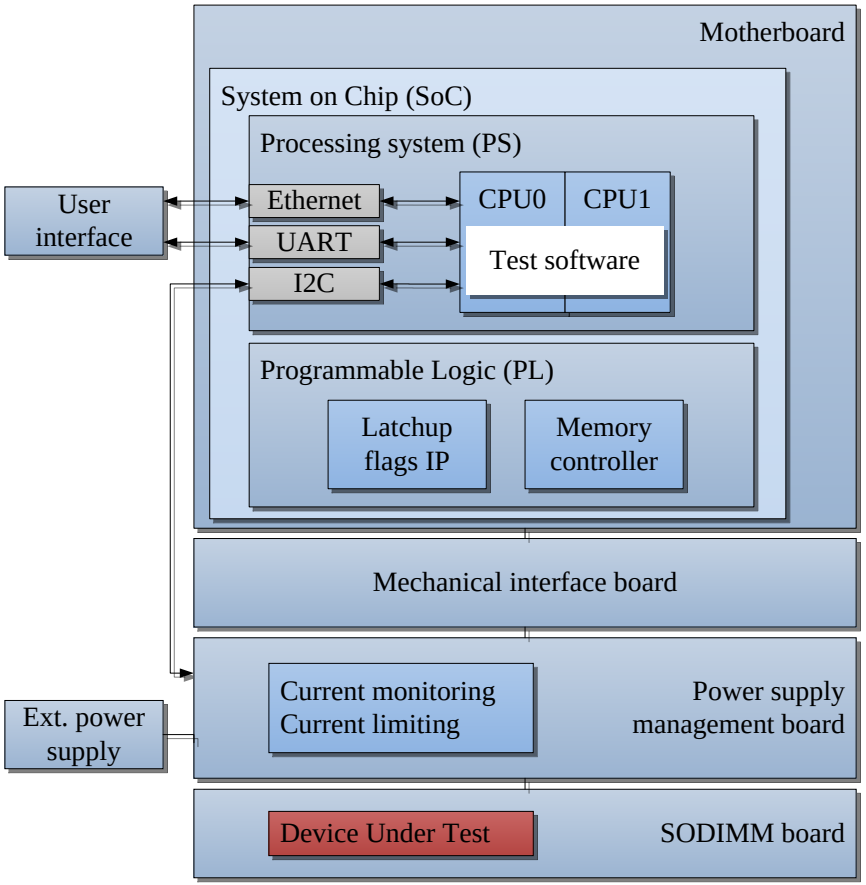
Sample	Memory type	Density	Max clock frequency	Supply voltage
A	DDR3	4 Gb	666 MHz	1.5 V
B	DDR3/L	2 Gb	933 MHz	1.35 / 1.5V
C	DDR3/L	4 Gb	800 MHz	1.35 / 1.5V

- **Sample preparation**
  - DUTs are mounted in **flip-chip** FBGA plastic package
  - The plastic is removed by acid attack to provide **access to the silicon substrate backside**



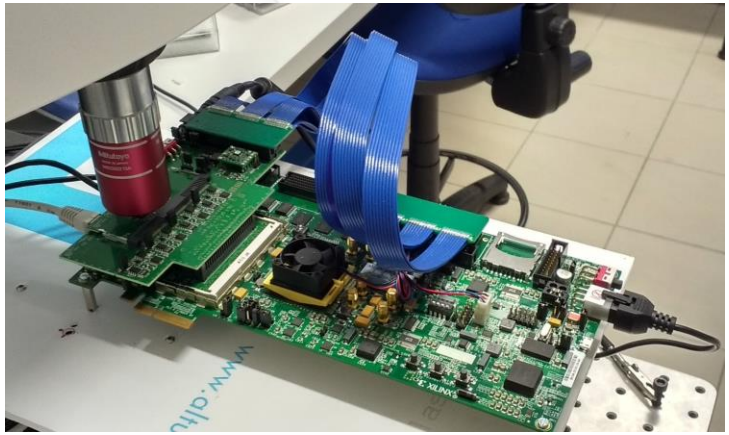
Test bench hardware overview

- **Test bench specifications**
  - Controlling **DDR3/L** SDRAMs under irradiation
  - DUTs clock frequency up to **800 MHz**
  - Up to **8 DUTs**
  - Parametric tests
    - Data retention time test
    - Power consumption monitoring
  - Functional tests
    - Read/write periodic cycles
    - Individual current limiting (**Delatcher**)

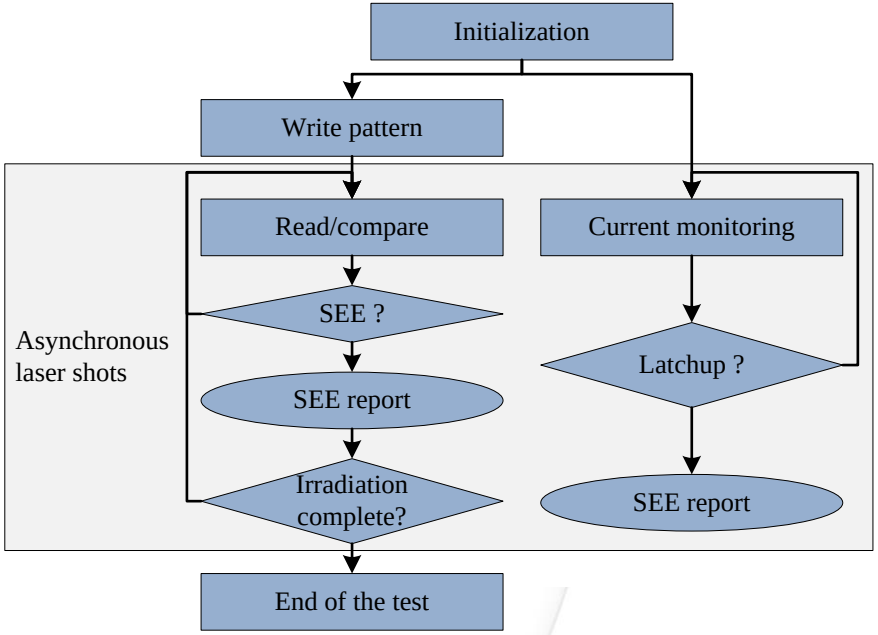


Experimental setup

- Laser testing facility
  - 2-photon laser facility of the IES lab of the University of Montpellier
  - Estimated TPA induced charge track FWHM : 0.7 µm



- Test procedure
  - Tests were performed at 400 MHz
  - Standard 64 ms auto-refresh interval was used (except for specific test modes)
  - Laser testing methodology
    - Starting with low pulse energies to observe non-destructive event
    - Gradual increase of laser energy to measure SEE threshold
    - Scan along Z axis to find the most sensitive depth
    - 2D mapping of SEU to descramble the memory organization



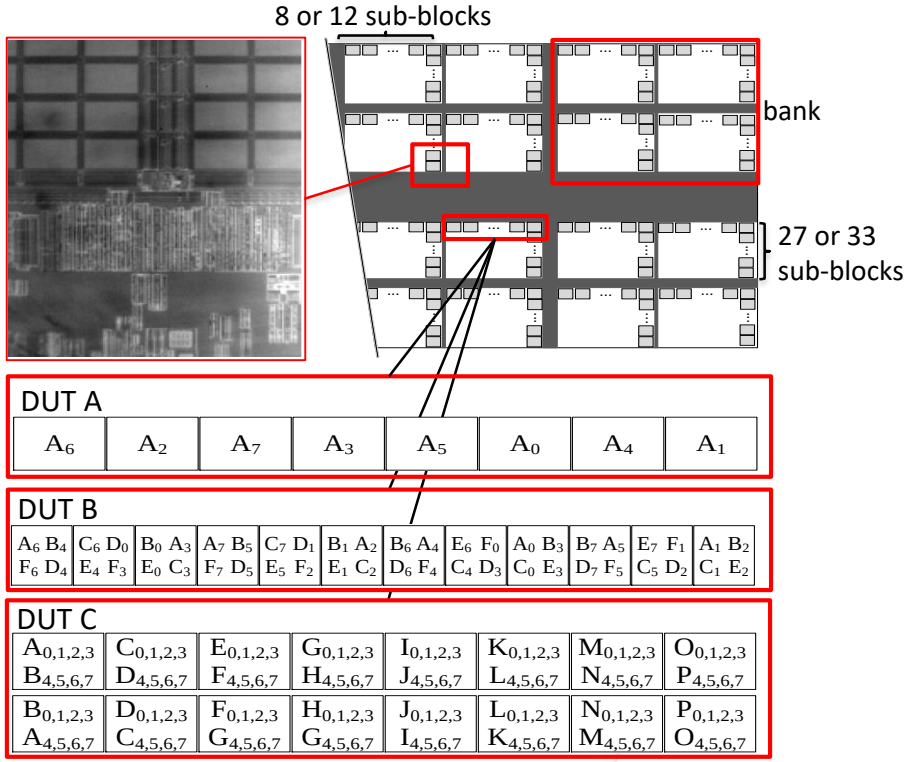
Memory organization

- **Memory array organization**
  - All DDR3 SDRAMs are divided in 8 **banks**
  - Banks in DUT A and C are divided in 4 **blocks**
  - Banks in DUT B are divided in 2 blocks
  - Each block is divided in **sub-blocks**

- **Data bits organization**
  - Descrambling : Correspondence between corrupted logical address and laser spot position
  - 3 tested devices exhibit very different scrambling strategies
    - For DUT A and B : the 8 bits of a same word are distributed into several sub-blocks
    - For DUT C, 4 bits of a same word are located in the same sub-block → More prone to MBU

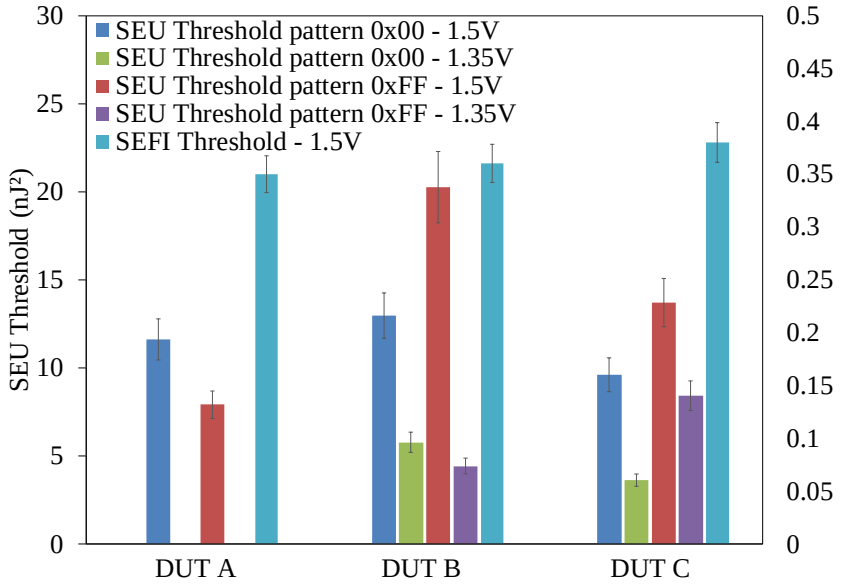
Sub-blocks description

DUT	Size X [µm]	Size Y [µm]	Sub-blocks /row	Sub-blocks /col	Estimated bit size [nm²]
A	100	50	8	33	10^4
B	68	51	12	33	10^4
C	72	43	8	27	5.10^3



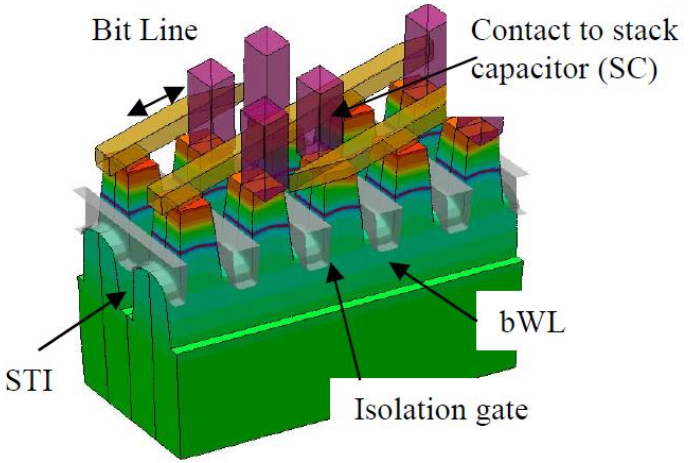
SEE laser energy thresholds

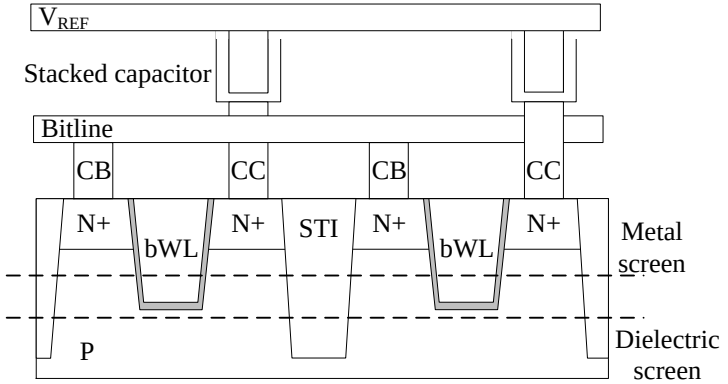
- **SEU and SEFI laser energy threshold measurement**
  - SEU_{TH} for 0x00 pattern and the $SEFI_{TH}$ are roughly the same for the 3 DUTs
  - SEU_{TH} for the 0xFF pattern differs by a factor 3 between DUT A and B
  - In low power mode SEU_{TH} is substantially lower than in normal power mode (≈ 60%)



SEU/SEFI thresholds comparison

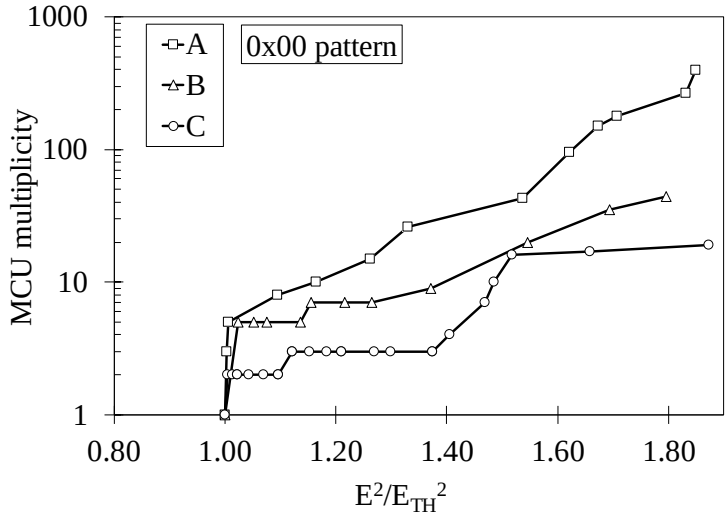
- **Unexpected result : Important ratio between SEU and SEFI thresholds**
  - Contrary to what was observed under heavy ions in previous works[1]
  - May be explained by the buried word-line (bWL) technology cell architecture
  - The small pitch of the bWLs (56 to 80 nm) may act as a partially reflecting virtual metal layer

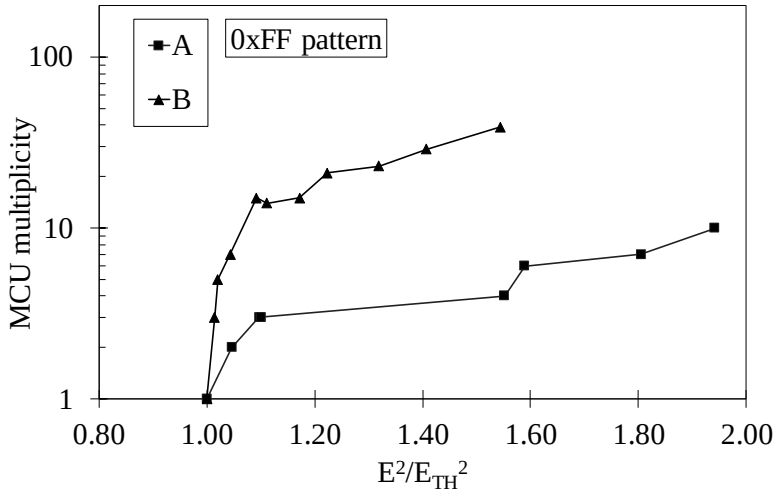




[1] *M. Herrmann et al, "New SEE and TID test results for 2-Gbit and 4-Gbit DDR3 SDRAM devices RADECS, 2013*

MCU multiplicity vs E^2/E_{TH}^2

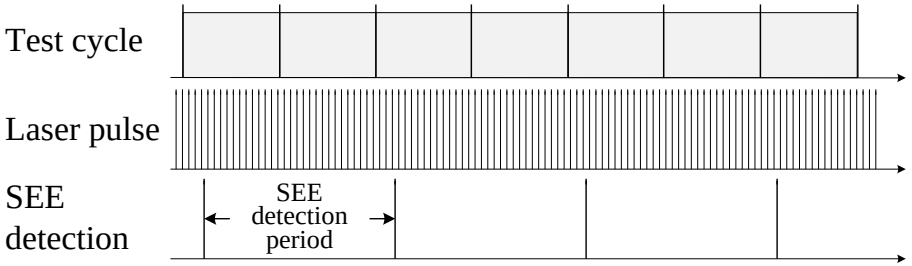




- Laser pulse energy increase ➔ MCU multiplicity increase
- 2 phenomena may explain the significant rise of the multiplicity
  - The effective laser spot size expands with energy
  - Total amount of charge generated by photoelectric effect increases with laser energy → diffusion towards adjacent cells
- These results may constitute behaviors under heavy ions with high LET or at grazing incidence
- Specific behavior of DUT C : with pattern 0xFF, damage threshold and correctable SEU threshold are nearly the same

Atypical upset occurrence - Observation

- **Observation** : Even above SEE threshold, sporadic events detection
  - Read cycle range : 1 to 10s (depending on the address range)
  - Laser pulse period : 100 ms (much larger than the refresh period)



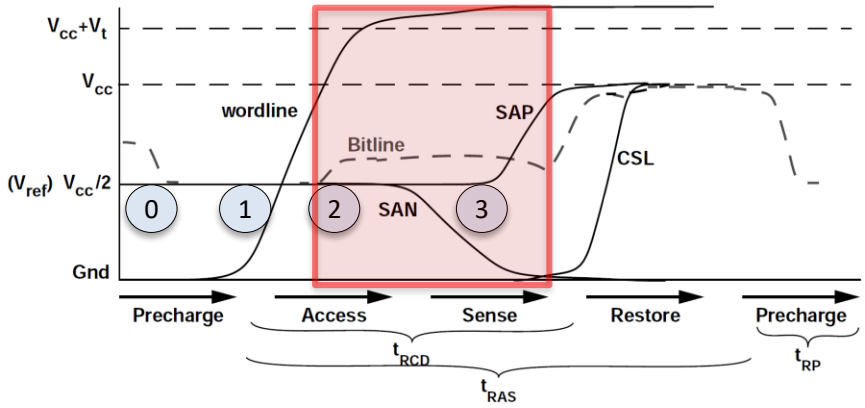
- Definition : **SEE detection period** is the SEE average time between two SEE observations

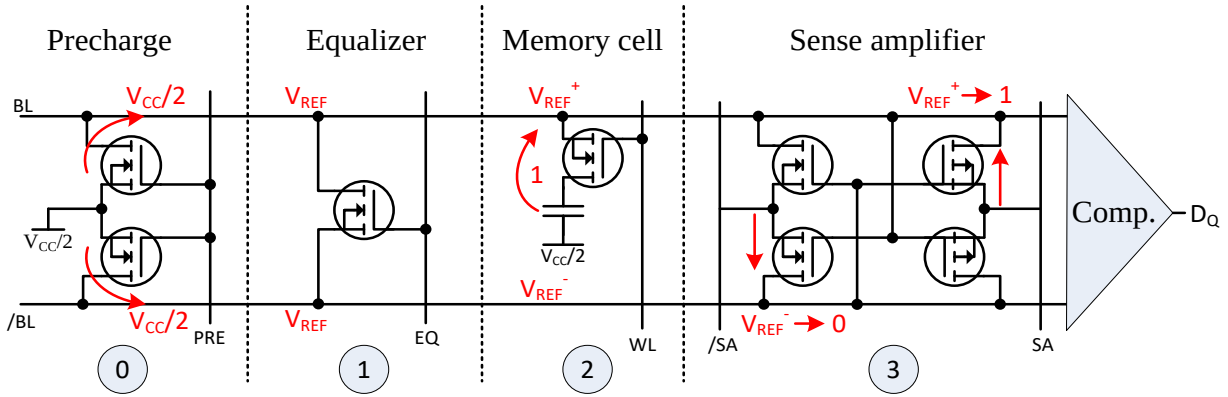
Atypical upset occurrence - Hypothesis

- **Hypothesis** : Existence of a critical time window for generating SEUs

- From previous works[1] [2]
  - **Bit-line upset** : bit-line disturbance occurring during a specific read or refresh cycle state when bit-lines are placed in a floating state

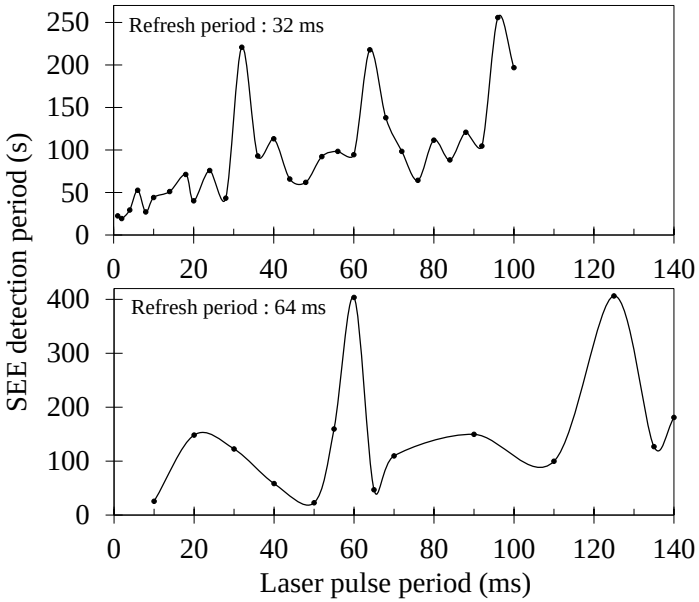
Critical time window for bit-line upset

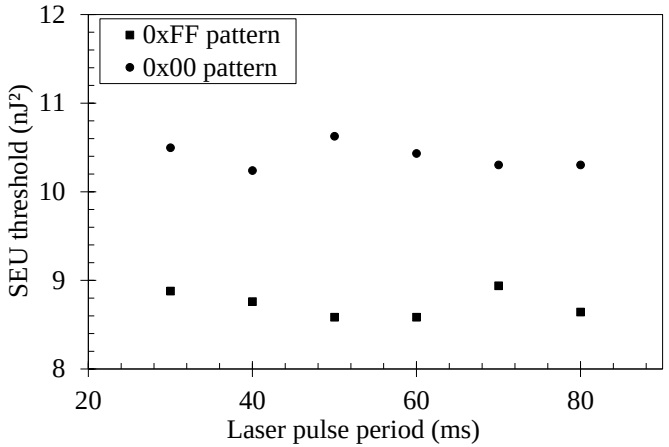




[1] *G. Schindlbeck, "Types of soft errors in DRAMs," RADECS, 2005*
[2] *A. Bougerol, F. Miller and N. Buard, "SDRAM Architecture & Single Event Effects Revealed with Laser", IOLTS 2008*

Evidence for bit-line upsets





- Highlight of the critical window for SEUs in the memory array using laser testing tool
  - SEU detection period vs laser pulse period (at $T_{REFRESH}$ = 32 and 64 ms)

  → Max of T_{SEE} when $T_{LASER} = k \times T_{REFRESH}$

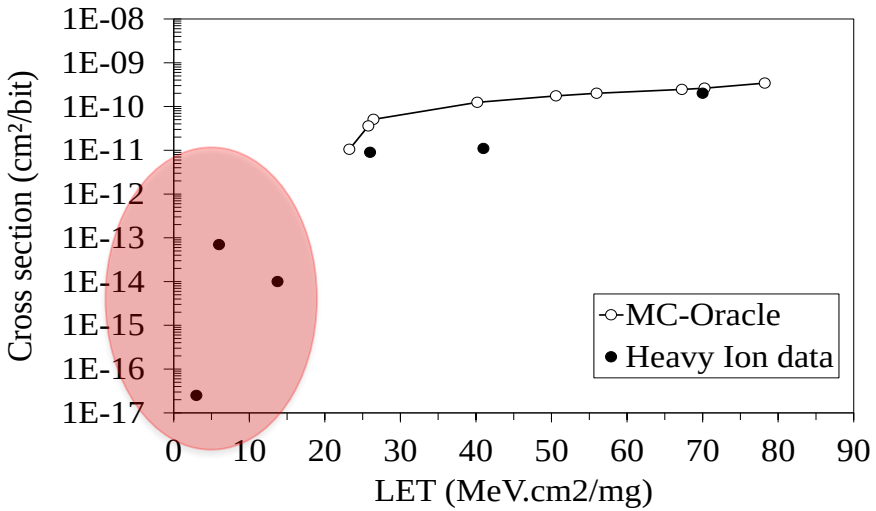
  ➔ **Existence of a vulnerable time window within each refresh cycle**

- SEU threshold vs laser pulse period supports this hypothesis
  - SEU_{TH} remains constant, regardless of the laser pulse period

  ➔ **These upsets are not induced by charge integration during several consecutive pulses**

Monte-Carlo Simulation

- Comparison of heavy ion SEU data obtained on DUT A in previous work[1] and Monte-Carlo simulation
  - Simulation of **only cell upsets** performed with MC-Oracle
  - Bits size and organization estimated from values obtained with IR camera and laser irradiation tool
  - We observe a good fit above 20 MeV.cm²/mg
- Lower part of the heavy ion data seems to confirmed the occurrence of bit-lines upsets
  - Lower threshold due to larger collecting nodes
  - Low cross-section due to the critical time window and refresh period ratio



[1] *K. Grürmann et al., "Heavy Ion Sensitivity of 16/32-Gbit NAND-Flash and 4-Gbit DDR3 SDRAM," 2012 REDW*

Conclusion

- Laser testing and analysis of SEE in DDR3 memory components from 3 different manufacturers using two-photon laser testing
- Specific test bench developed and validated during experimental TID, HI and laser test campaigns
- Laser testing results
  - Extraction of physical and technological information (bit, array organization)
  - SEU/SEFI thresholds measurement and comparison
  - MCU multiplicity vs laser energy
  - Demonstration of the occurrence of bit-line upsets
- Laser good complementarity tool before HI experiments and for extracting important information for SEE assessment

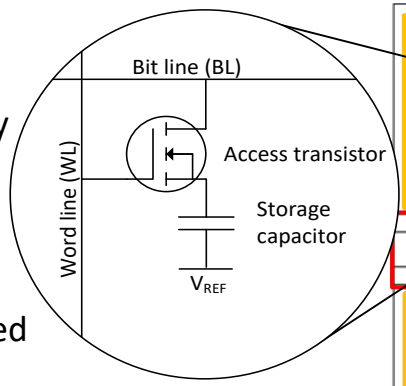
Thank you for your attention

Backup slides

DRAM principles

DRAM Cell

- DRAM : Dynamic Random Access Memory
- 1T/1C Cell
- Binary information stored in a capacitor connected to an access transistor
- Capacitor leakage current induces the need to periodically refresh information
- Volatile : Information are lost after power cycling

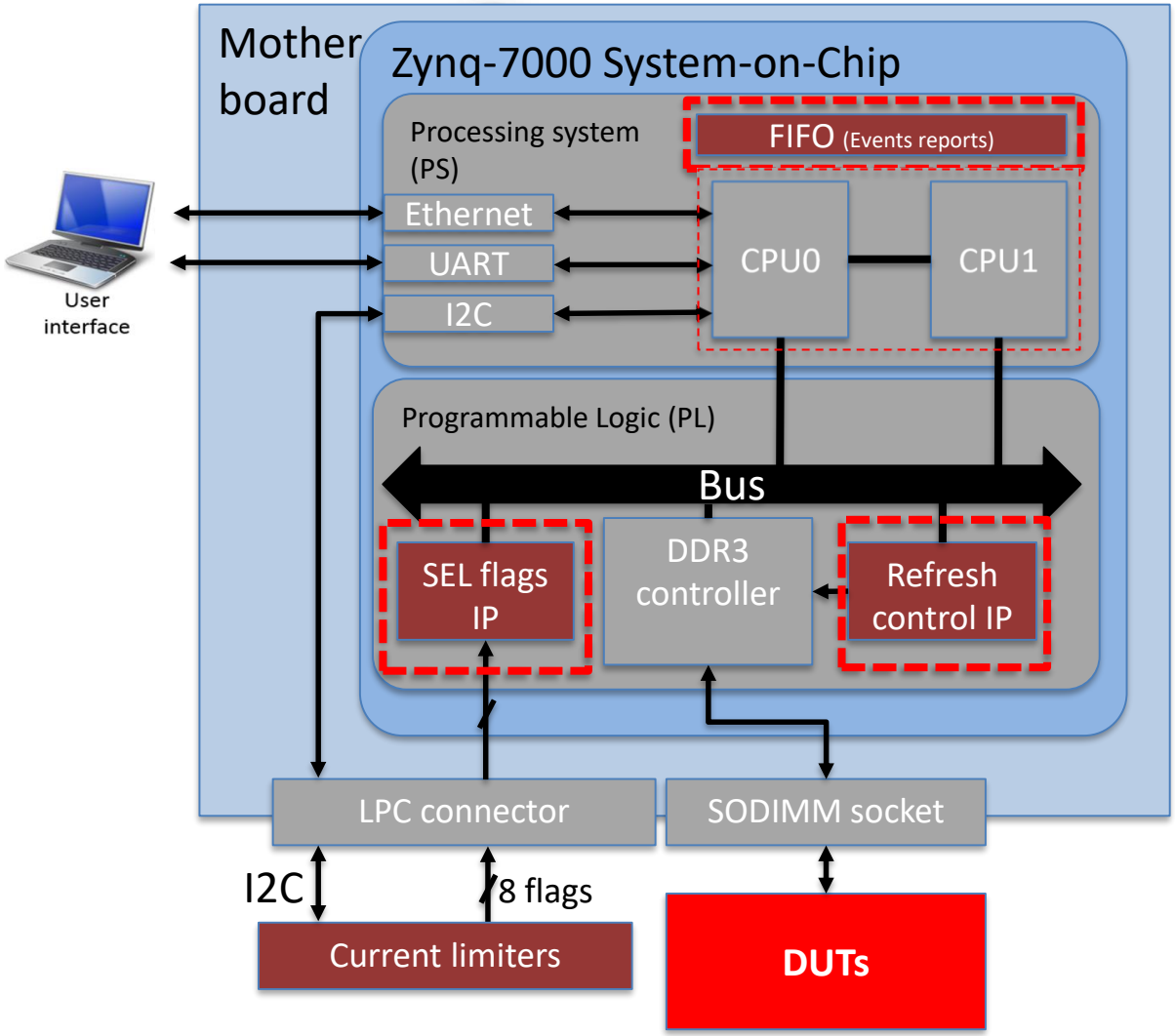


Memory physical organization

- Common standard (JEDEC)
- Manufacturer dependent elements:
  - Technology node
  - Memory cells scrambling (physical distribution of the cells on the chip)
  - Capacitor technology
  - Peripheral circuitry

Standard DRAM architecture

Hardware design architecture



SEL flags IP

- Stores latchup flags in a register
- "OR" logic gate asserts an output signal when a latchup is detected

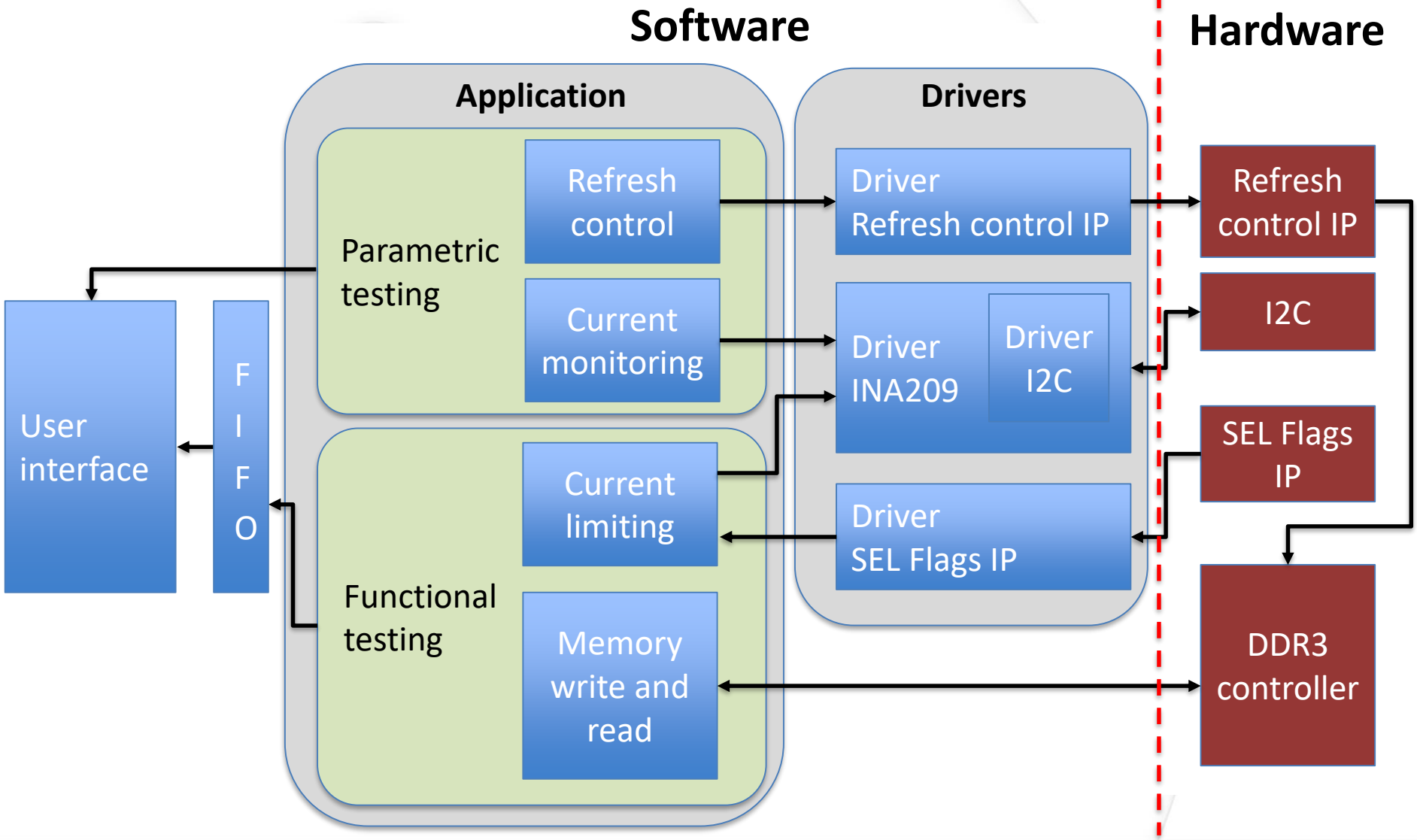
Refresh control IP

- User control of the Refresh command
- Aim : **Data retention time measurement**
- Configurable time interval

FIFO

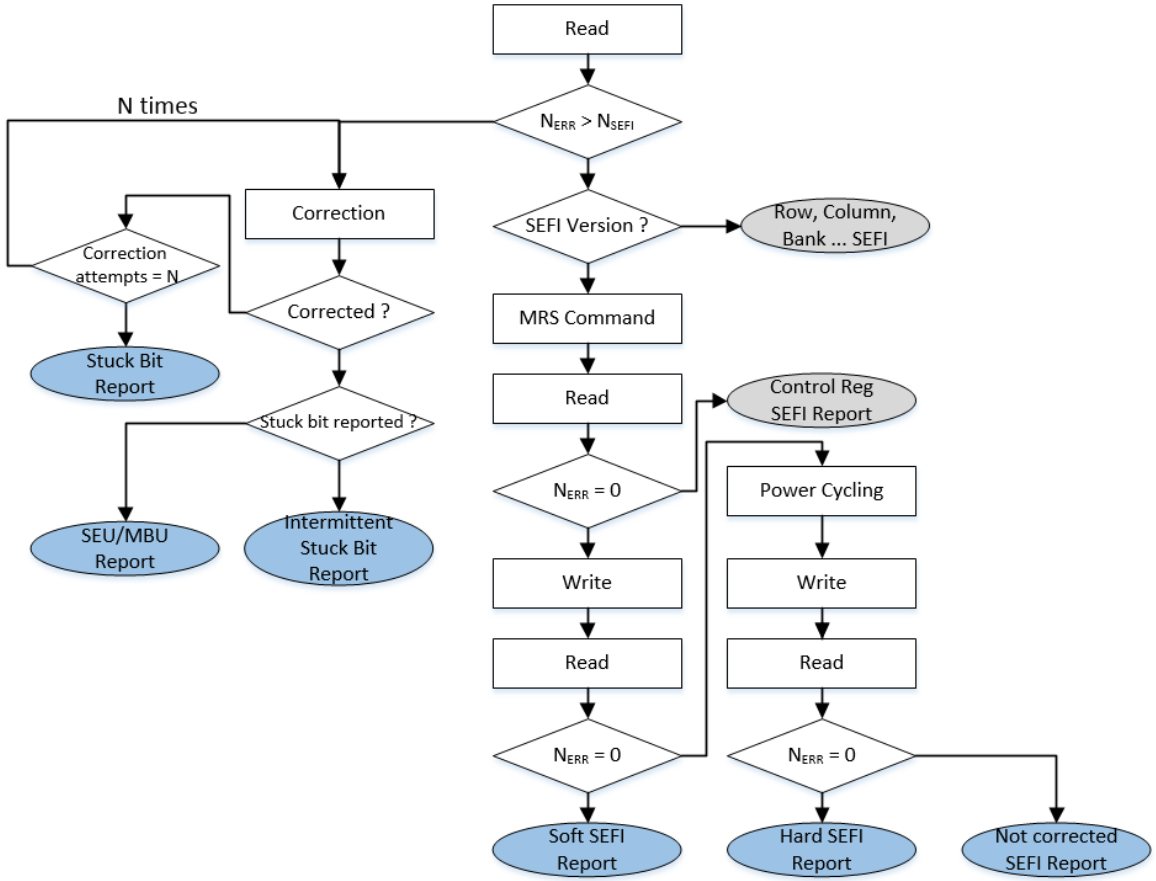
- Software CPU shared memory
- Stores events reports

Software Architecture



Single-Event Effects

- Algorithm proposed to classify Single-Event Effects :
  - SEL monitoring runs in parallel
  - Identify SEU, Multiple upsets, stuck bits and different types of SEFIs
  - Reveal errors in control registers
- The algorithm should evolve depending on the test results



Software development

- Use of the two processors available in the Zynq module
  - CPU0 functions
    - Parse ethernet user commands
    - Control test program sequences
    - Unqueue events reports stored in a FIFO
  - CPU1 functions
    - Manage DUTs read/write accesses
    - Check/correct SEUs
    - Report events in a FIFO
- CPU1 pre-processing
  - In order to prevent FIFO flooding
    - Add MBUs detection and correction functions
    - Add SEFIs detection functions
- Shared memory stores test parameters and commands sent from CPU0 to CPU1